Mixed Signal Neural Decoder

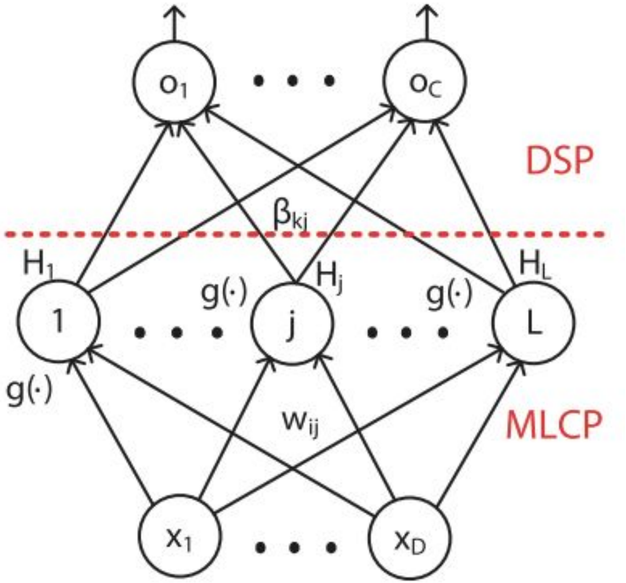
Rebekah Zhao, Anil Bilgin, Cody Yang

Objectives

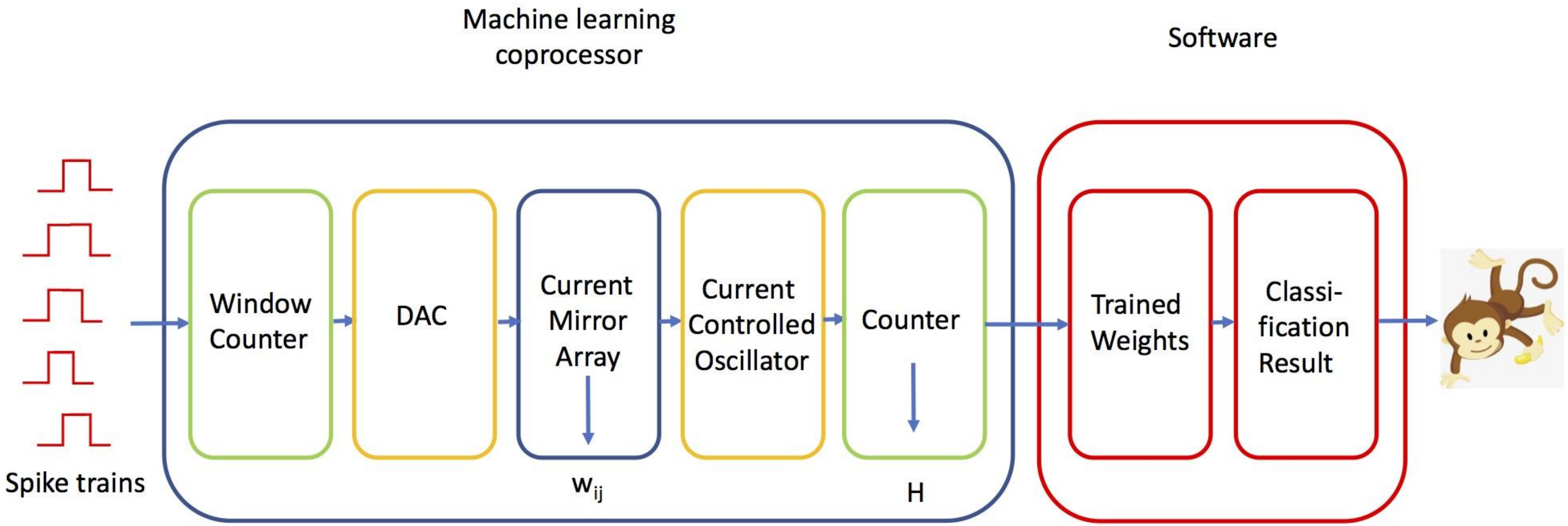
- Design an implantable, power-efficient ASIC to perform neural decoding via Machine Learning
- Existing solutions
  - PC based decoding: very high accuracy, power hungry and not implantable
  - Separate neural decoding from neural recording: high wireless data transmission rate
  - FPGA: consumes more power than ASIC, not implantable
  - VLSI circuit: Achieves high accuracy, but some blocks are less efficient than their analog equivalents

Our Solution

- Extreme Learning Machine (ELM) algorithm
  - Specific type of SLFN, where input weights and biases can be random (and not trained) if the activation function is infinitely differentiable.
- Our assumptions & Implementation details
  - Take in sorted spike trains as inputs from multiple channels
  - Implement hidden layer with mixed-mode IC
  - Implementing the output layer of the ELM in software (MATLAB)
- What we would demo
  - Schematic of circuit design
  - Simulation results of algorithm
  - Layout of circuit design



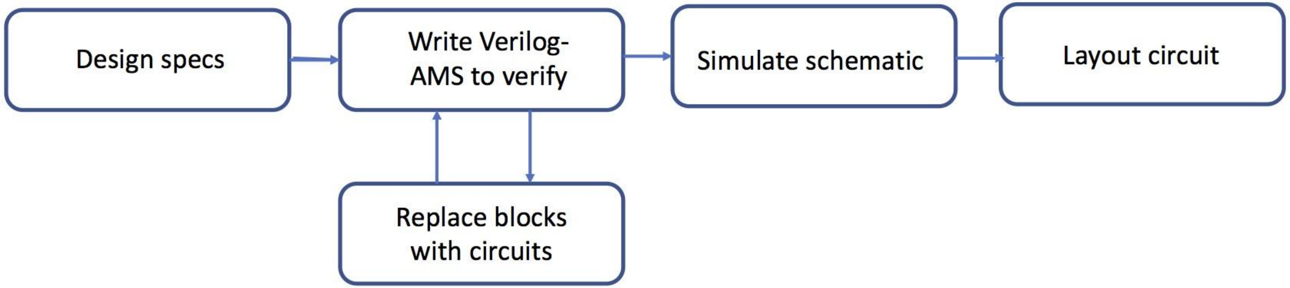
Design Diagram



No components need to be purchased, simulation based project

Tools

- Verilog-AMS: a tool to simulate mixed-signal circuits
- Cadence: circuit simulation and layout

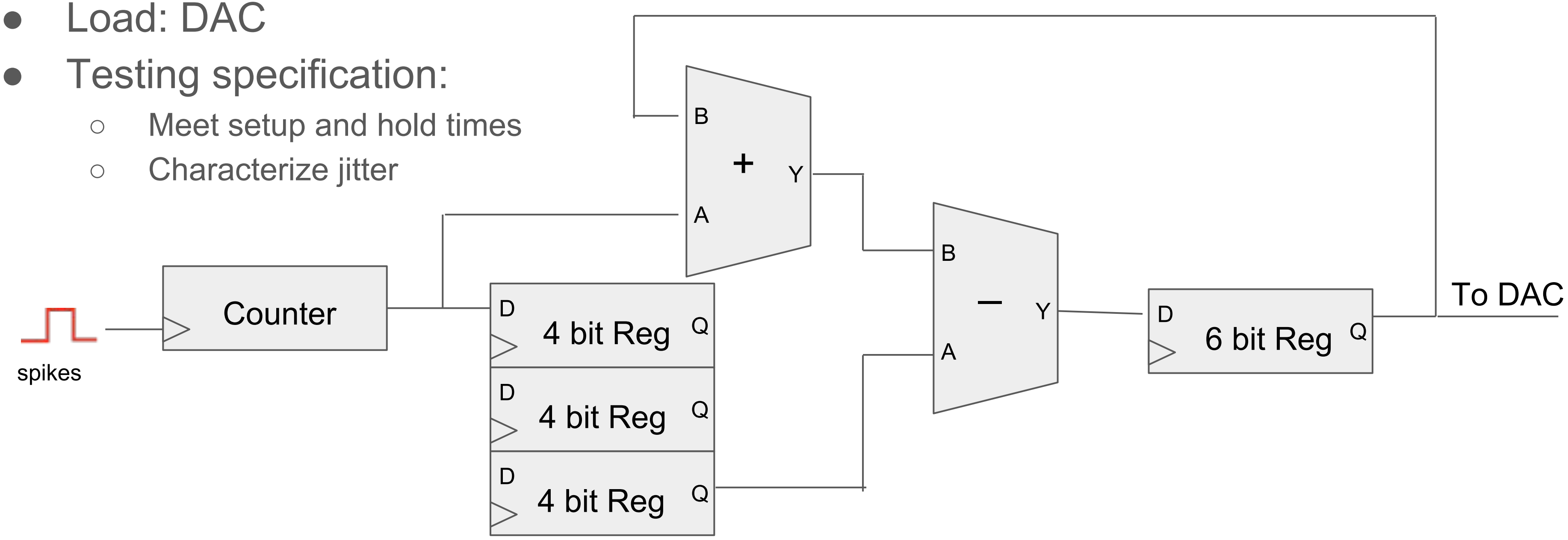


Neural data

- **Data type:** Premotor cortex (PMd) and Primary Motor Cortex (M1) recording from a sequential reaching task of monkey
- **Data content:** Spike sorted data from 67 channels per pre-set time bins for each reaching task, the instantaneous position, velocity and acceleration.
- **Data source:**
    - Matthew G. Perich, Patrick N. Lawlor, Konrad P. Kording, Lee E. Miller (2018); Extracellular neural recordings from macaque primary and dorsal premotor motor cortex during a sequential reaching task. CRCNS.org. http://dx.doi.org/10.6080/K0FT8J72

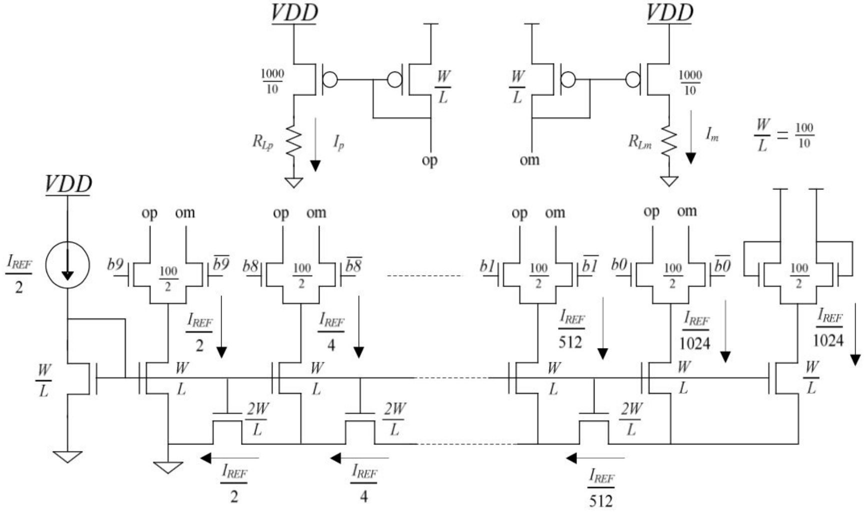
Window Counter

- Input: Spike train (digital signal)
- Output range: 6 bits
- Load: DAC
- Testing specification:
  - Meet setup and hold times
  - Characterize jitter

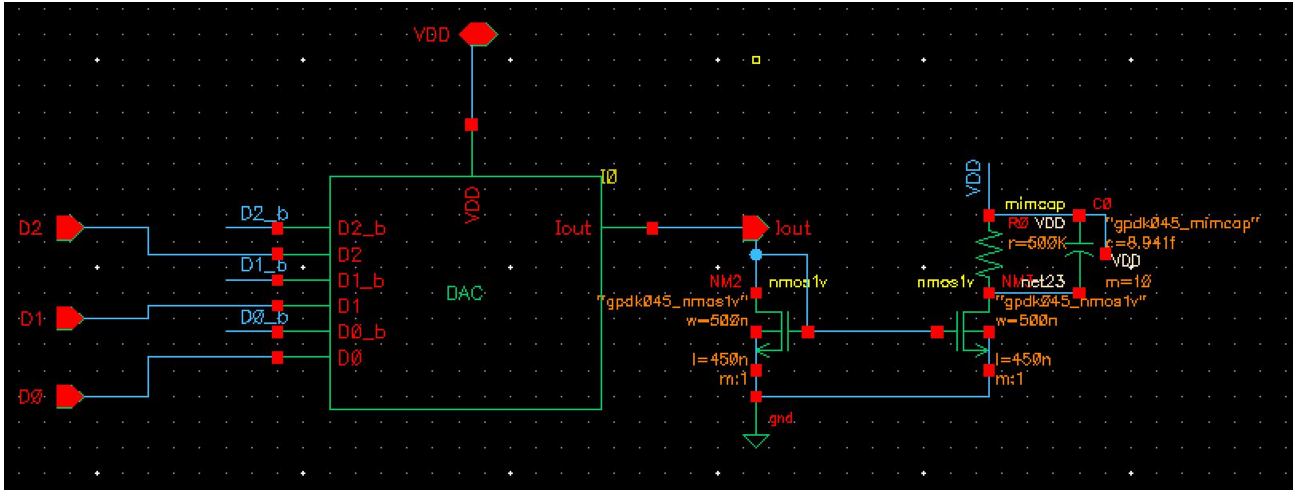


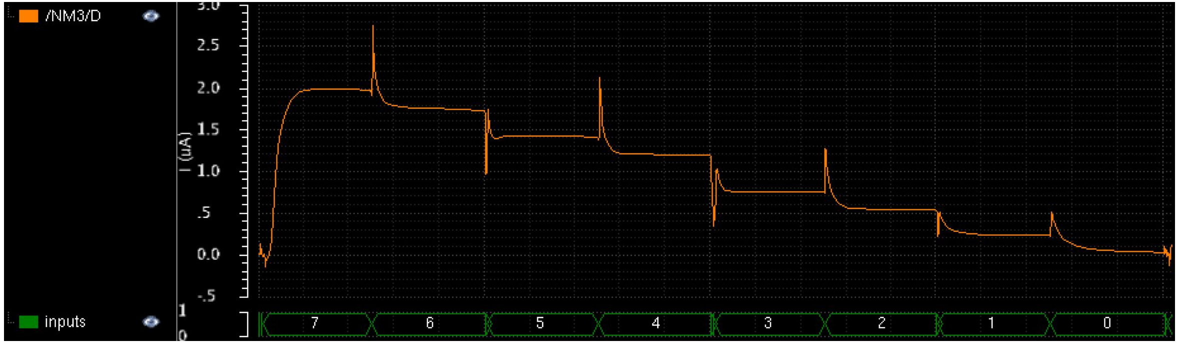
Digital to Analog Converter (DAC)

- Input: spike count from window counter (6 bit)
- Output range: 1nA - 63nA
- Load: current mirror array
- Testing specification: differential nonlinearity (DNL) ± 3 bits



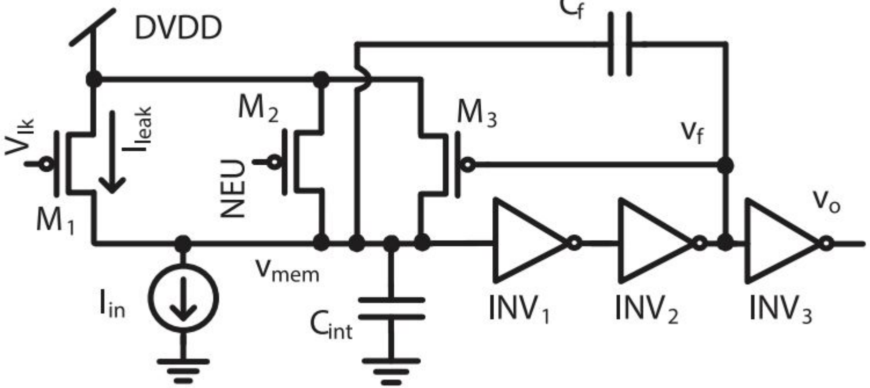
Testing circuit and result



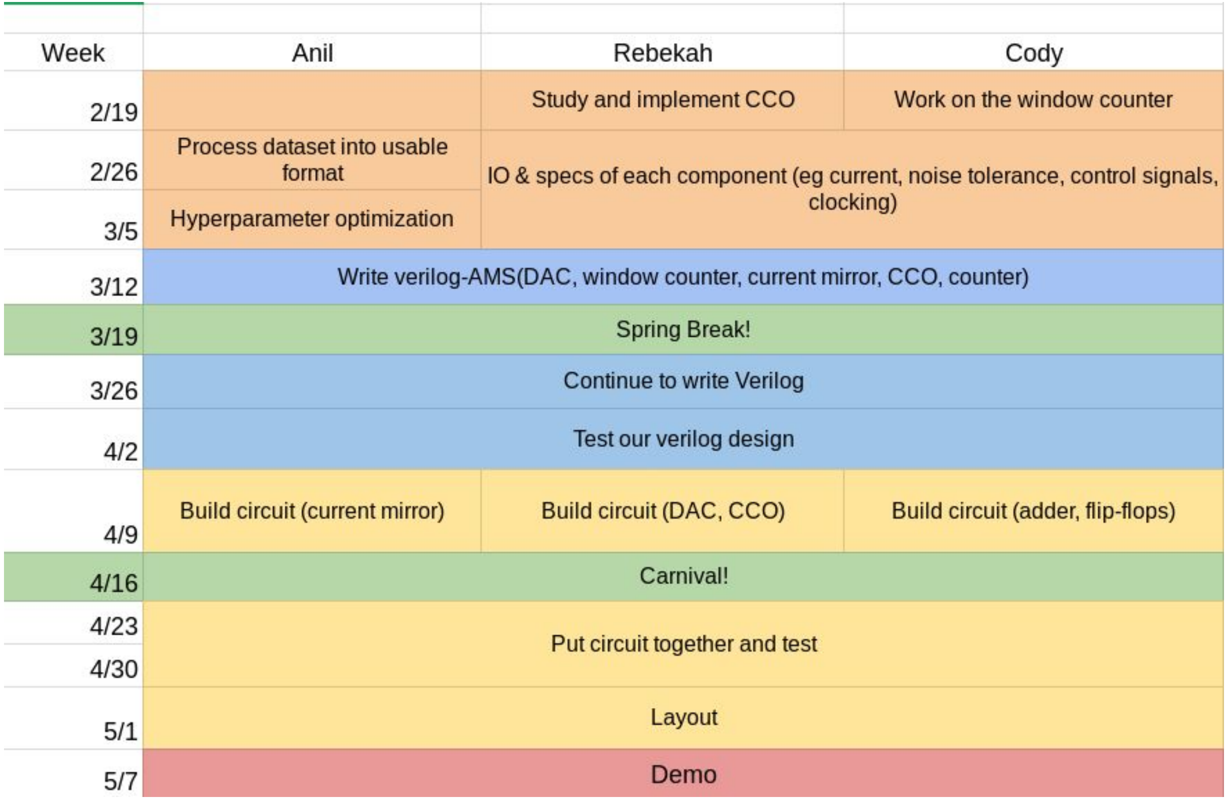


Current Controlled Oscillator

- Input: current mirror array
- Load: counter
- Output: pulse frequency modulated signal with the frequency proportional to input current
- Testing specification: charging and discharging dynamic; jitter (<0.1%)



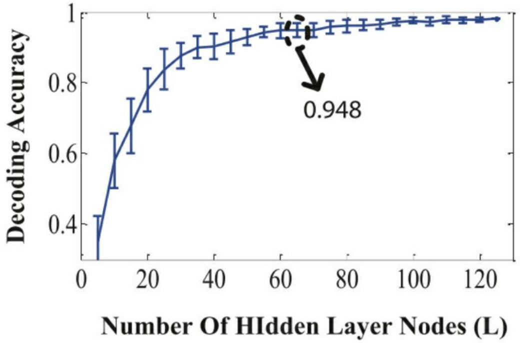
Projected timeline

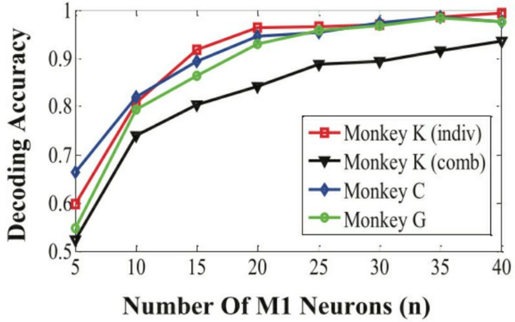


Week	Anil	Rebekah	Cody
2/19		Study and implement CCO	Work on the window counter
2/26	Process dataset into usable format	IO & specs of each component (eg current, noise tolerance, control signals, clocking)	
3/5	Hyperparameter optimization		
3/12	Write verilog-AMS(DAC, window counter, current mirror, CCO, counter)		
3/19	Spring Break!		
3/26	Continue to write Verilog		
4/2	Test our verilog design		
4/9	Build circuit (current mirror)	Build circuit (DAC, CCO)	Build circuit (adder, flip-flops)
4/16	Carnival!		
4/23	Put circuit together and test		
4/30			
5/1	Layout		
5/7	Demo		

Testing plan

- Target specifications:
  - Power consumption - 0.4 mW/mm^2 upper limit
  - Decoding accuracy target ~ 90%
- Testing:
  - Cross validation with 80% of our data while training
  - Test our design with the remaining 20% to measure decoding accuracy
  - Measure power consumption per unit area using Cadence





Risk factors

- Ultra Low power design
  - Subthreshold operation
  - Noise and jitter
- Testing complexity
  - Data conversion between tools (from discrete data to circuit input, from circuit output to discrete data)
  - Simulating device mismatch